Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A ferroelectric memory device comprising:

an interlayer dielectric layer;

a protection adhesion layer on the interlayer dielectric layer;

a buried contact extending through the protection adhesion layer and the interlayer dielectric layer;

a lower electrode on a portion of the protection adhesion layer adjacent to the buried contact and on the buried contact;

a ferroelectric layer covering the lower electrode and the protection adhesion layer; and

an upper electrode overlapping with the lower electrode and covering the ferroelectric layer.

2. (Original) A ferroelectric memory device according to Claim 1 wherein the buried contact comprises:

an upper buried contact portion comprising a barrier pattern extending from the lower electrode through the protection adhesion layer; and

a lower buried contact portion extending from the barrier pattern through the interlayer dielectric layer.

3. (Original) A ferroelectric memory device according to Claim 1 wherein the protection adhesion layer comprises titanium oxide layer (TiO_2).

4. (Original) A ferroelectric memory device according to Claim 2 wherein the barrier pattern is selected from the group consisting of TiN, TiAlN, $TiSi_x$, TiSiN, TaSiN and TaAlN.

5. (Original) A ferroelectric memory device according to Claim 1 wherein the ferroelectric layer is selected from the group consisting of PZT[Pb(Zr, Ti)O_3], $PbTiO_3$, $SrTiO_3$, $BaTiO_3$, $PbLaTiO_3$, (Pb, La) (Zr, Ti)O_3, BST[(Ba, Sr)TiO_3], $Ba_4Ti_3O_{12}$, $SrBi_2Ta_2O_9$ and $Bi_4Ti_3O_{12}$.

6. (Original) A ferroelectric memory device according to Claim 1 wherein the lower electrode and the upper electrode are selected from the group consisting of ruthenium (Ru), platinum (Pt), rhodium (Rh), osmium (Os), palladium (Pd), ruthenium oxide (RuO_x), iridium oxide (IrO_x) and platinum oxide (PtO_x), rhodium oxide (RhO_x), osmium oxide (OsO_x) and palladium oxide (PdO_x).

7. (Original) A ferroelectric memory device according to Claim 1 wherein the buried contact is selected from the group consisting of tungsten, aluminum, copper and polysilicon doped or undoped with impurities.

8. (Original) A ferroelectric memory device according to Claim 1 wherein the lower electrode comprises one of a plurality of lower electrodes, wherein the upper electrode overlaps at least two of the plurality of lower electrodes.

9. (Original) A ferroelectric memory device according to Claim 8 further comprising:

an upper interlayer dielectric layer covering the ferroelectric layer and the upper electrode; and

a plate line electrically connected to the upper electrode through the upper interlayer dielectric layer.

10. (Original) A ferroelectric memory device according to Claim 8 further comprising:

a strip line on the upper interlayer dielectric layer; and

an upper metal interlayer dielectric layer covering the strip line, wherein the plate line is electrically connected to the upper electrode through the upper metal interlayer dielectric layer and the upper interlayer dielectric layer.

Claims 11-25 (Canceled).